USBDL1 [FD/G/GA/GN/GNA/A16]

General (1st generation)

The data logger *USBDL1* can acquire signals from its 10 voltage inputs, 5 digital inputs (e.g. frequency signals), and serial input (e.g. GPS signals), and output these signals to a PC. These signals can also be saved onto a USB stick. Additionally, the USBDL1 can also receive and transmit signals from up to two CANs (Controller Area Network) and one LIN (Local Interconnect Network) subbus. Additionally, the *USBDL1 FD* supports also up to two CAN FD. The *USBDL1 G* has a 60-ms-GPS-receiver integrated. The *USBDL1 GA* has a 60-ms-GPS-receiver integrated and two voltage outputs. And the *USBDL1 A16* can acquire up to 16 voltage signals.

Before using the data logger, it must first be set up by defining a parameter set with the PC program TEMES (which requires a PC with a USB 2.0 port and at least Windows XP), and then by writing this parameter set to a USB 2.0 stick. After making the measurement, the USB stick can be put again into a PC, and the stored data can be written to a PC file for further processing.

Figure 1: Data logger USBDL1.

Sample Rate

The input signals can be recorded at two different sample rates. The first sample rate is the basic sample rate which can be set to integer multiples of 100 µs, and the second sample rate is an integer multiple of the basic sample rate. The slower second sample rate is 1 to 256 times larger and should also not be larger than 15 s. Note, that a high sample rate of 10 kHz is only working for simple/limited configurations.

The data logger has a further cycle which runs at a user adjustable rate (with a default value of 10 ms). This cycle is used for CAN signals and calculated signals.

Finally, the USBDL1 has a cycle with a low priority which runs at a fixed rate of 10 ms.

Voltage Input Signals

The data logger *USBDL1* can acquire up to 10 voltage signals with a resolution of 12 bits. And the data logger *USBDL1 A16* can acquire up to 16 voltage signals with a resolution of 12 bits. These signals can be measured within the voltage range from 0 V to 5.12 V where 0 V corresponds to bit value 0, and where 5 V corresponds to bit value 64000 (= 16 × 4000). However, the signals can lie within the range from -30 V to 30 V without a negative impact on other signals. The internal impedance of each voltage input is greater than 10 MΩ.

Each voltage signal input connector has a pin to supply a preamplifier with the operating voltage (decreased by about 1 V) of the data logger.

The voltage signals are sampled with 10 kHz and represented by the average value over a period of the corresponding sample rate.

If at most 5 voltages are acquired, the voltage signal can optionally be further smoothed with a 4fold averaging. And if at most 14 voltages are acquired, the voltage signal can optionally be further smoothed with a 2fold averaging instead.

Voltage input signals can optionally be linearized via a table look-up during the calculation cycle. For this purpose, user defined characteristic curves are used. Look-up values for input values, which lie between two sample points, are obtained by linear interpolation.

Digital Input Signals

The data logger has five channels for digital signals:

Frequency Signal: The input voltage level (TTL, CMOS) may lie within the range from 0 V to 20 V. The frequencies to be measured may lie in the range from 0.1 Hz to 100 kHz. Note that the sum over all five input frequencies must not be greater than 100 kHz. The digital signal can be triggered either with the raising edge or the falling edge of the input signal, and is represented by the average value over a period of the sample rate.

Switch State: Depending on the voltage level of the digital input, the digital signal is taken either as bit value 0 or as bit value 1. This signal type can be used for markers or to reset counter readings (see *calculated signals*).

Pulse Width (only the first three digital inputs): The pulse width to be measured may lie in the range from 1 µs to 546 ms. The signal resolution is from 8.333 ns to 8.533 µs (in 9 steps). The digital signal is represented by the average value over a period of the sample rate.

Counter: The 16-bit wrap-around counter is incremented by one after each pulse.

Serial Ports

The data logger has two serial ports. The first serial port is used for the communication between data logger and host PC (*RS232*). The 2nd serial port can be used by one of the following items:

GPS receiver: The 2nd serial port can be used to receive NMEA sentences of a GPS receiver. The NMEA receiver supports the messages GGA, VTG, RMC and ZDA. Following unsigned 16-bit signals can be extracted: Message counter, time (resolution: 0.01 s), timestamp (hhmmss with a resolution of 2 s), date (yyMMdd), speed (resolution: 0.01 kph), height (resolution: 0.1 m; lowest height: 500 m below sea level), number of visible satellites. Following signed 32-bit signals can be extracted: longitude, latitude (with a resolution of 1/600000 degree).

F6 protocol: The 2nd serial port can be used to acquire up to 16 signals via the f6 protocol.

LIN subbus: The 2nd serial port can be used to access a LIN subbus via the optionally available adapter *LIN719/SICO(LOG)*. See also section *LIN*.

CAN

The data logger can be connected to two CANs (Controller Area Network). Each of the two CAN channels has the ability to receive or to transmit up to 32 CAN messages (with either 11-bit or 29-bit message identifiers). The messages are refreshed during the calculation cycle.

Input signals are embedded within a received message. To extract them, following properties are supported: *start bit* within a message, *bit length* (max. 32 bits), *data type* (*unsigned* or *signed*) and *byte order* (*Intel* or *Motorola*).

The data logger hardware (physical layer) is compatible to a high speed CAN (which is usually run at 125 kBit/s, 500 kBit/s or 1 MBit/s). An optional adapter integrates the data logger with a low speed CAN (which is usually run at 83.3 kBit/s, 100 kBit/s or 125 kBit/s).

Note, that each of the two ends of a high speed CAN must be terminated (typically with a 120 Ω resistor between *CAN_H*-wire and *CAN_L*-wire).

If the CAN signals can be assigned freely, then following rules should be followed in order to reduce the computational complexity:

- Choose Intel as byte-alignment
- Choose 16-bit or 32-bit as data type
- DWORD-align the start bit: 0, 32. If not possible, then WORD-align the start bit: 0, 16, 32, 48. (If not possible, then try BYTE-alignment: 0, 8, 16, 24, 32, 40, 48, 56.)
- Avoid further linear transformations

CAN FD

The USBDL1 does not support a CAN FD. The USBDL1 FD on the other hand supports additionally up to two CAN FD. See section USBDL1 FD for further information.

Another method to access a CAN FD is a CAN FD router which maps the CAN FD messages to a CAN, like PCAN Router FD from PEAK-System Technik GmbH.

LIN

The 2nd serial port of the USBDL1 can be used over the optionally available adapter LIN719/SICO(LOG) to access a LIN subbus (Local Interconnect Network). It can be configured to work either as a master control unit or as a slave control unit. The USBDL1 can receive or transmit up to 8 LIN messages. The messages (to be received or to be transmitted) are refreshed during the calculation cycle.

Input signals are embedded within a received message. To extract them, following properties are supported: start bit within a message, bit length (max. 32 bits), data type (unsigned or signed) and byte order (Intel or Motorola). Multiplex signals are only supported for message reception (and not for transmission). However, the USBDL1 ignores bus-sleep-requests and wake-up-signals.

As master control unit, the USBDL1 supports one schedule table with up to 16 identifier-delay-entries (where the delay must be an integer multiple of the calculation cycle time).

If the LIN signals can be assigned freely, then following rules should be followed in order to reduce the computational complexity:

- Choose Intel as byte-alignment
- Choose 16-bit or 32-bit as data type
- DWORD-align the start bit: 0, 32. If not possible, then WORD-align the start bit: 0, 16, 32, 48. (If not possible, then try BYTE-alignment: 0, 8, 16, 24, 32, 40, 48, 56.)
- Avoid further linear transformations

Calculated Signals

The data logger supports operations with signal values. For this purpose the signal values are treated as signed 32-bit integer values with little-endian (= Intel) byte order. Following operations are already built in the firmware: constant value; basic arithmetic (sum, difference, product, ratio); bit manipulations (AND, OR, XOR, mirror bits, byte order change from Intel to Motorola and vice versa); comparisons (=, <, ≤); condition (use signal s_1 if condition is true, otherwise use signal s_2); delay (e.g. for derivation or signal filtering); counter operations (e.g. for 32-bit-counters or for integration).

More complex operations can be obtained by using the result of a single operation as an operand for following operations.

Power Control

The data logger should never be powered off by suddenly breaking the supplying voltage while it is recording (indicated by the *REC* LED). Instead, it should be powered off either manually with the power slider, or automatically by removing the power control signal from connector *ON*.

By turning off the power slider, while the data logger is recording, first a stop event is created, and then (after this stop event has been processed) the data logger is powered off after the file cache is empty (because the data logger is no longer recording).

When using the *ON* connector to control the power state of the data logger, the power slider should be left turned off.

An ongoing recording after the stop event can be stopped forcibly by turning the *REC* slider off.

Recording Control

Note that a measurement can only be erased with holding the buttons *B1* and *B2* down after the *REC* slider has been turned off. If there exists a measurement, then the *User LED* is lit (or inverted) for about two seconds, and when it automatically extinguishes (with unchanged button states), also the measurement is erased.

Trigger Conditions

The data logger supports up to four trigger conditions. If one condition changes from not satisfied to satisfied, it generates either a start or a stop event. The condition is always a comparison of an input signal with a constant threshold value. Calculated signals can be used to obtain a more complex trigger.

Real Time Clock

The data logger has a built-in real time clock. A 32-bit time stamp is derived from current date and time with a resolution of 1 s. This time stamp represents the seconds from the beginning of the year 1970 to the actual point in time.

If, however, the real time clock is not available, the time stamp is set to zero. Note, that the real time clock is not automatically adjusted for daylight saving changes.

Technical Data

Property	Description
Power supply:	8 V to 16 V DC
Current consumption without USB stick (@ 12 V DC):	ca. 60 mA
Quiescent current (= Power Off @ 12 V DC):	ca. 150 µA
Sample rate:	1 ms (with limited abilities: 100 µs) or slower
CAN bus:	ISO11898-1 compliant
USB:	USB 2.0 Full Speed
Box size without plugs, sockets, buttons and sliders:	73 mm × 60 mm × 26 mm
Weight:	0.140 kg

PC Software

The data logger can be set up with the PC software TEMES. TEMES requires a PC with a USB 2.0 port and at least Windows XP. The current version can be downloaded from the Internet (http://tellert.de/?product=TEMES).

Further functions of TEMES are:

- **Online-Calibration:** The voltage input signals can be calibrated either at one known point (offset adjustment) or at two known points (two-point calibration).
- **Online-View:** The online-view displays a curve chart of the current signal values in the upper part of the window. The lower part of the window is used to display these values as numbers in physical units.
- **Saving Measurements:** The measurements, which are captured by the USBDL1, can be stored to a PC file. After storing the data, the measurement can directly be displayed as a curve chart.
- **Exporting Measurements:** A measurement can (via a provided and documented DLL interface) be exported to ASCII, MDF3, M, SCE, JL and R file format. This DLL also allows programmers to read TEMES measurement files without knowing the internal file structure (http://tellert.de/?product=til).

Following TEMES functions require an optional available single-PC license:

- **Import of ASCII files:** Measurements can be imported from ASCII files.

Scope of Supply

The delivery of a data logger USBDL1 includes:

- USBDL1 box
- USB stick
- 4-pin-cable for power supply (12 V DC) and CAN with open wire ends
- PC-connection cable with either a USB plug or a 9-pin SUB-D-socket
- PC-software (TEMES, which requires a computer with a USB 2.0 port and at least Windows XP)

Optional Accessories

General accessories:

- Power transformer (Euro plug; 100-230 V AC; 50-60 Hz)
- Low speed CAN adapter *LCC719* (to connect the USBDL1 to a low speed CAN)
- Power-off delay *POD8*

Accessories for digital input:

- Hall effect sensor *HS-M10X1* (to detect passing magnets)
- Hall effect sensor *FPS* (to measure the frequency of steal teeth wheels)
- Preamplifier *PP1* for AC-coupled signals (for magnetic sensors)

Accessories for voltage input:

- Differential Input Amplifier *DIA1/DIA2*
- DC-bridge amplifier *DCBA1ME/DCBA2ME*
- Temperature sensor *PT100M/PT1000M*
- NTC temperature sensor *NTC10K* (operating point 25 °C) and *NTC2K* (operating point 66 °C) for temperatures from –40 °C to 150 °C
- Thermal sensor amplifier *TH1M/TH2M*
- Galvanically isolated thermal sensor amplifier *TH16MI/CAN* (16 channels, multiplexed)

Accessories for the RS232 connector:

- GPS receiver *HS10G/HS16G/HS25N* or *GPS10G/GPS16G/GPS25N*
- External displays *ED*, *ED4*, *ED9*, and *ED12*
- LIN adapter *LIN719/SICO(LOG)*

USB Stick

The USB 2.0 stick (whose size should be no more than 2 TiB) has to be formatted either with one partition of FAT16 (with 512 bytes per sector) or with one partition of FAT32 (with 512 bytes per sector).

When a fresh USB stick is inserted, the USBDL1 first initializes the USB stick (which takes usually around 10 minutes). During this phase also the file

\TELLERT\SICOLOG\CONFIG.TSF

is created, and communication is impossible. The initialization phase must also not be interrupted, otherwise the stick needs to be formatted again, and the initialization must be started again.

As soon as measured data is available, the stick must not be defragmented.

A USB stick needs to be *ejected* before it is unplugged from the PC (in order to keep the FAT16 or FAT32 file system healthy). TEMES has a checkbox for ejecting a USB stick automatically (see the corresponding mass storage dialog boxes), otherwise the USB stick needs to be ejected manually (e.g. with the context menu of the Windows Explorer).

Note that the *REC* LED should be unlit if you remove the power from connector *POWER/CAN*. See section *Power Control* for further information.

For performance reasons, it is recommendable to use at least a USB 3.0 stick.

Performance

24-hours-recordings onto a SanDisk Ultra Fit 32 GB USB 3.0 stick, without loosing a sample, are listed as follows (Note, that the overhead of one sample is two bytes in these cases):

Sample rate [ms]	Number of 16-bit channels	Size [GiB]	Speed [KiB/s]
0.1	3	6.4	78
0.2	8	7.2	88
0.3	12	7.0	85
0.4	18	7.6	93
0.5	23	7.7	94
1	51	8.4	102

When the USBDL1 is too slow to write the signals onto the USB stick in time, the USBDL1 stops the measurement and restarts the measurement with an additional timestamp and a mention in the TEMES variable *Measurement.M1.exceptions*. The duration of lost samples (between measurement stop and start) is usually maximal 4 seconds.

The settings of working online TEMES charts are listed as follows:

Sample rate [ms]	Number of 16-bit channels		Speed [KiB/s]
0.2	1		9.8
0.3	2		13
0.4	3		15
0.6	4		13
0.7	5		14
0.8	6		15
0.9	7		15
1.1	8		14
2	15		15
2.1	16		15
5	38		15
10	77		15

Encryption

The USBDL1 does not support the SICOLOG encryption. But there is a variant of the USBDL1 available (on request), namely the *USBDL1 E-Edition*, which supports encryption with a key length of 56 bits.

More Information (Internet)

The USBDL1 homepage is available at:

http://www.tellert.de/?product=usbdl1

Pin Assignment

The sockets and plugs of the USBDL1 are manufactured by *Binder* and parts of *Binder Series 719*. The socket pins (in front view) are numbered clockwise starting with the first pin after 12 o'clock position. The plug pins are numbered correspondingly anti-clockwise. The first pin is respectively labeled at the solder side (back view).

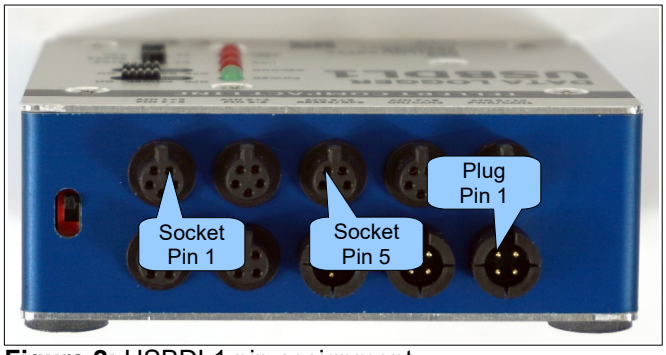

Figure 2: USBDL1 pin assignment.

PWR/CAN1: This plug supplies the data logger with voltage and connects the data logger to CAN1.

Pin	Assignment	Old Wire Color	Wire Color
1	Supplying voltage U_B (8 V to 16 V DC inverse-polarity protected)	Red	Brown
2	Ground	Brown	White
3	CAN_L (CAN1)	Black	Blue
4	CAN_H (CAN1)	Orange	Black

ON/CAN2: This plug provides a power control input and connects the data logger to CAN2.

Pin	Assignment	Old Wire Color	Wire Color
1	Power control input (6 V to 16 V DC)	Red	Brown
2	Ground	Brown	White
3	CAN_L (CAN2)	Black	Blue
4	CAN_H (CAN2)	Orange	Black

RS232/GPS: This plug provides two serial ports.

Pin	Assignment	9-pin SUB-D plug of host PC
1	TX1	Pin 2
2	Ground	Pin 5
3	RX1	Pin 3
4	U_B – 0.5 V or TX2	RS232 switch up: U_B – 0.5 V RS232 switch down: TX2
5	RX2	

AIN1+2, ..., AIN9+10: These sockets provide inputs for the voltage input signals.

Pin	Assignment U_L
1	U_B – 0.5 V
2	Ground
3	Analog input 1 (or 3/5/7/9)
4	Analog input 2 (or 4/6/8/10)
5	5.12 V reference voltage (max. 50 mA for AIN1+2...AIN9+10)

FIN1+2: This socket provides a connection to the first two digital (frequency) signals.

Pin	Assignment
1	U_B – 0.5 V
2	Ground
3	Digital input 1 connected over 100 kΩ to 5 V
4	Digital input 2 connected over 100 kΩ to 5 V

FIN3-5: This socket provides a connection to the last three digital (frequency) signals.

Pin	Assignment
1	Digital input 5 connected over 100 kΩ to 5 V
2	Ground
3	Digital input 3 connected over 100 kΩ to 5 V
4	Digital input 4 connected over 100 kΩ to 5 V

USBDL1 FD (1st generation)

The USBDL1 FD supports additionally up to two CAN FD. Each CAN FD channel is limited to 8 Mbps, 2 KiB RAM and no support for remote frames.

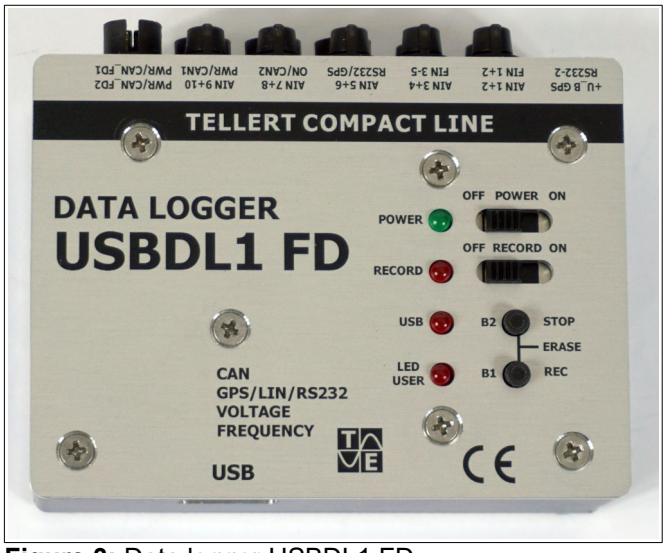

Figure 3: Data logger USBDL1 FD.

Each of the two CAN FD channels has the ability to receive or to transmit up to 31 CAN FD messages (with either 11-bit or 29-bit message identifiers). The messages are refreshed during the calculation cycle.
Input signals are embedded within a received message. To extract them, following properties are supported: *start bit* within a message, *bit length* (max. 32 bits), *data type* (*unsigned* or *signed*) and *byte order* (*Intel* or *Motorola*).

Note, that each of the two ends of a CAN FD must be terminated (typically with a 120 Ω resistor between *CAN_H*-wire and *CAN_L*-wire).

If the CAN FD signals can be assigned freely, then following rules should be followed in order to reduce the computational complexity:

- Choose Intel as byte-alignment
- Choose 16-bit or 32-bit as data type
- DWORD-align the start bit: 0, 32, … If not possible, then WORD-align the start bit: 0, 16, 32, 48, ... (If not possible, then try BYTE-alignment: 0, 8, 16, 24, 32, 40, 48, 56, ...)
- Avoid further linear transformations

Deviating Technical Data

Property	Description
Current consumption without USB stick (@ 12 V DC):	ca. 60 mA + 10 mA per used CAN FD channel
Box size without plugs, sockets, buttons and sliders:	80 mm × 60 mm × 26 mm
Weight:	0.150 kg

Additional Pin Assignment

PWR/CAN_FD1: This plug supplies the data logger with voltage and connects the data logger to CAN_FD1.

Pin	Assignment	Old Wire Color	Wire Color
1	Supplying voltage U_B (8 V to 16 V DC inverse-polarity protected; internally connected with pin 1 of PWR/CAN1)	Red	Brown
2	Ground (internally connected with pin 2 of PWR/CAN1)	Brown	White
3	CAN_L (CAN_FD1)	Black	Blue
4	CAN_H (CAN_FD1)	Orange	Black

PWR/CAN_FD2: This plug supplies the data logger with voltage and connects the data logger to CAN_FD2.

Pin	Assignment	Old Wire Color	Wire Color
1	Supplying voltage U_B (8 V to 16 V DC inverse-polarity protected; internally connected with pin 1 of PWR/CAN1)	Red	Brown
2	Ground (internally connected with pin 2 of PWR/CAN1)	Brown	White
3	CAN_L (CAN_FD2)	Black	Blue
4	CAN_H (CAN_FD2)	Orange	Black

USBDL1 G (1st generation)

The data logger USBDL1 G has, additionally to the USBDL1, the GPS module *GPS16G* integrated.

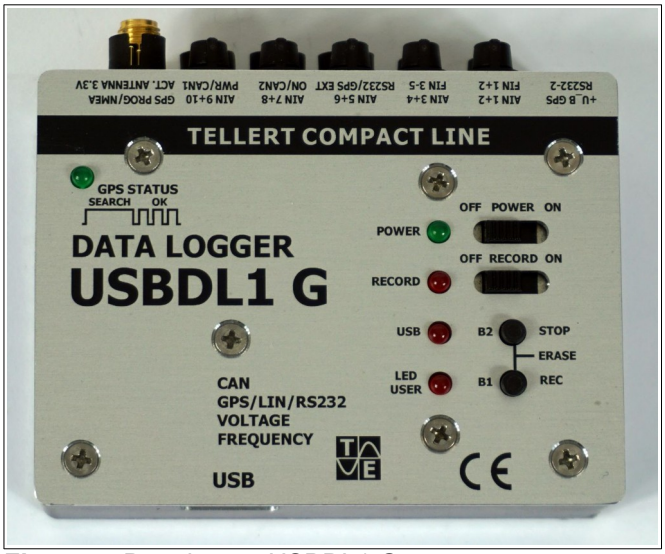

Figure 4: Data logger USBDL1 G.

Deviating Technical Data

Property	Description
Current consumption without USB stick (@ 12 V DC):	ca. 60 mA + 50 mA if the GPS module is powered

Box size without plugs, sockets, buttons and sliders:	80 mm × 60 mm × 26 mm
Weight:	0.152 kg
Refreshing rate:	16⅔ Hz
NMEA output:	VTG, GGA and ZDA data sentences with 115200 baud.
Status LED:	**Green permanent light:** no GPS data. **Green blinking light:** valid GPS data.
GPS module:	NEO-M8N (from u-blox)
Presetting for the GPS module:	SBAS deactivated; ≤ 9 satellites; *portable* platform (speed ≤ 1116 kph; altitude speed ≤ 180 kph; altitude ≤ 12 km)

GPS module (according to u-blox):

Property	Description
Chip set:	U-blox NEO-M8N
Sensitivity:	Tracking & Navigation: -164 dBm Reacquisition: -159 dBm Cold Start: -147 dBm Hot Start: -156 dBm
First sample:	After 1 s (after 30 s in the worst case)
Speed accuracy:	0,05 m/s (50 % @ 30 m/s)
Direction accuracy:	0,3° (50 % @ 30 m/s)
Position accuracy:	2.5 m (CEP, 50 %, 24 hours static, -130 dBm, > 6 SVs)

See also
https://www.u-blox.com/en/product/neo-m8-series

Additional Pin Assignment

GPS PROG/NMEA: This connector provides a connection to the serial NMEA output, and provides a connector for (re)programming the GPS module.

Pin	Assignment
1	Serial transmitting pin to transmit the NMEA data sentences with 115200 baud.
2	Ground
3	Serial receiving pin to (re)program the GPS module
4	Not connected
5	Not connected

LNA: The LNA connector is of type SMA and connects the USBDL1 G with an active GPS antenna. The LNA connector is temporarily short circuit protected. The active GPS antenna is supplied with 3.3 V DC.

USBDL1 GA (1st generation)

The data logger USBDL1 GA extents the data logger USBDL1 G with two 12-bit-D/A-converter-channels. The output voltage lies within the range from 0 V to 5 V. Each output has an internal impedance of 1 kΩ. Note that the update rate of the D/A converter is limited to 0.3 ms or larger.

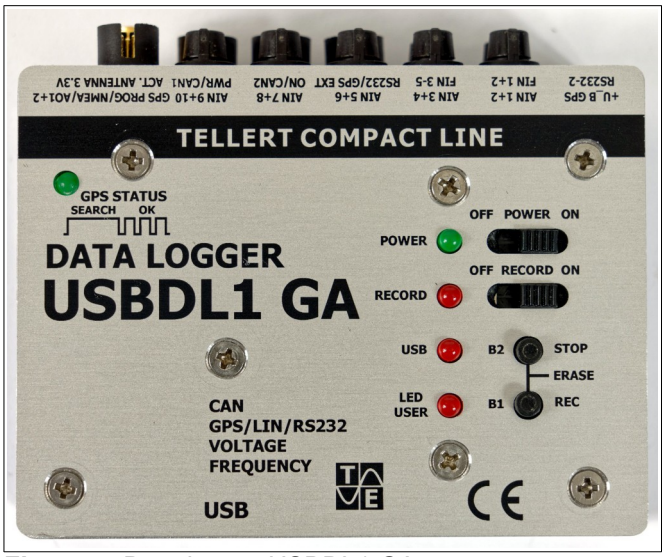

Figure 5: Data logger USBDL1 GA.

Deviating Technical Data

Property	Description
Current consumption without USB stick (@ 12 V DC):	ca. 60 mA + 50 mA if the GPS module is powered
Box size without plugs, sockets, buttons and sliders:	80 mm × 60 mm × 26 mm
Weight:	0.159 kg
Refreshing rate:	16⅔ Hz
NMEA output:	VTG, GGA and ZDA data sentences with 115200 baud.
Status LED:	**Green permanent light:** no GPS data. **Green blinking light:** valid GPS data.
GPS module:	NEO-M8N (from u-blox)
Presetting for the GPS module:	SBAS deactivated; ≤ 9 satellites; *portable* platform (speed ≤ 1116 kph; altitude speed ≤ 180 kph; altitude ≤ 12 km)

Deviating Pin Assignment

GPS PROG/NMEA: This connector provides a connection to the serial NMEA output, and provides a connector for (re)programming the GPS module.

Pin	Assignment
1	Serial transmitting pin to transmit the NMEA data sentences with 115200 baud.
2	Ground
3	Serial receiving pin to (re)program the GPS module
4	Analog output 1: 0...5.12V, R_i = 1kΩ, $T_{update} \geq 0.3$ms
5	Analog output 2: 0...5.12V, R_i = 1kΩ, $T_{update} \geq 0.3$ms

USBDL1 GN (1st generation)

The data logger USBDL1 GN has, additionally to the USBDL1, the GNSS module *GNSS25N* integrated.

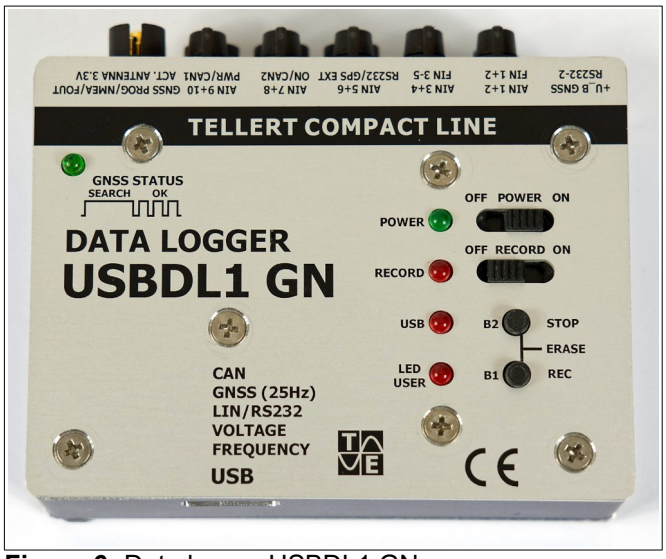

Figure 6: Data logger USBDL1 GN.

Digital Output Signal

If digital channel 1 and 2 are not used as signal input, they can be used as signal output:

Frequency signal ($f_{Min} < f_{Max}$): The output voltage level (TTL, CMOS) is either 0 V or 5 V. The frequency output may lie within the range from 2 Hz to 100 kHz.

PWM signal ($f_{Min} = f_{Max}$): The output voltage level (TTL, CMOS) is a frequency signal 0 V or 5 V with a frequency of f_{Min}, and a duty cycle depending on the signal source and assignment.

Switch state ($f_{Min} > f_{Max}$): The output voltage level (TTL, CMOS) is either 0 V or 5 V depending on the signal source and assignment.

Deviating Technical Data

Property	Description
Current con-ssssumption without USB stick (@ 12 V DC):	ca. 60 mA + 70 mA if the GPS module is powered
Box size without plugs, sockets, buttons and sliders:	80 mm × 60 mm × 26 mm
Weight:	0.156 kg
Refreshing rate:	25 Hz
NMEA output:	VTG, GGA and ZDA data sentences with 115200 baud.
Status LED:	**Green permanent light:** no GNSS data. **Green blinking light:** valid GNSS data.
GPS module:	NEO-M9N (from u-blox)

GPS module (according to u-blox):

Property	Description
Chip set:	u-blox NEO-M9N
Sensitivity:	Tracking & navigation: -167 dBm Reacquisition: -160 dBm Cold/warm start: -148 dBm Hot start: -159 dBm
First sample:	After 2 s (and in worst case after 42 s)
Speed accuracy:	0.05 m/s (50 % @ 30 m/s)
Direction accuracy:	0.3°
Position accuracy:	2.5 m CEP

See also
https://www.u-blox.com/en/product/neo-m9n-module

Additional Pin Assignment

GPS PROG/NMEA: This connector provides a connection to the serial NMEA output, and provides a connector for (re)programming the GPS module.

Pin	Assignment
1	Serial transmitting pin to transmit the NMEA data sentences with 115200 baud.
2	Ground
3	Serial receiving pin to (re)program the GPS module
4	Digital output 1 (= frequency output 1)
5	Digital output 2 (= frequency output 2)

LNA: The LNA connector is of type SMA and connects the USBDL1 G with an active GPS antenna. The LNA connector is temporarily short circuit protected. The active GPS antenna is supplied with 3.3 V DC.

USBDL1 GNA (1st generation)

The data logger USBDL1 GNA replaces the two digital outputs of the data logger USBDL1 GN with two 12-bit-D/A-converter-channels. The output voltage lies within the range from 0 V to 5 V. Each output has an internal impedance of 1 kΩ. Note that the update rate of the D/A converter is limited to 0.3 ms or larger.

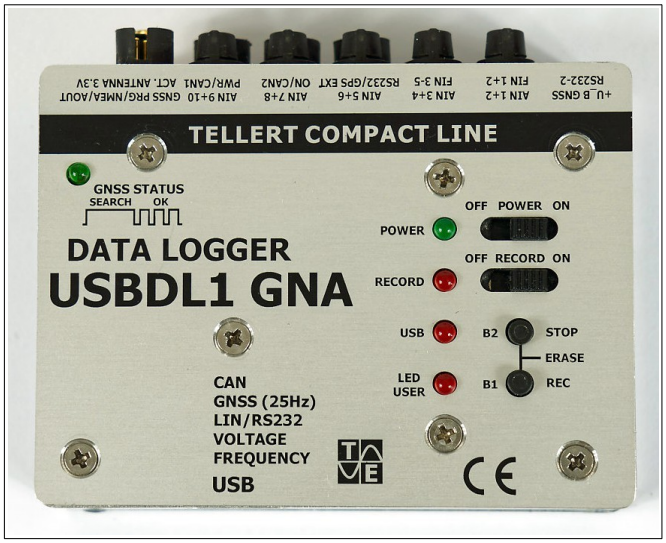

Figure 7: Data logger USBDL1 GNA.

Deviating Technical Data

Property	Description
Current consumption without USB stick (@ 12 V DC):	ca. 60 mA + 70 mA if the GPS module is powered
Box size without plugs, sockets, buttons and sliders:	80 mm × 60 mm × 26 mm
Weight:	0.160 kg
Refreshing rate:	25 Hz
NMEA output:	VTG, GGA and ZDA data sentences with 115200 baud.
Status LED:	**Green permanent light:** no GNSS data. **Green blinking light:** valid GNSS data.
GPS module:	NEO-M9N (from u-blox)

Deviating Pin Assignment

GPS PROG/NMEA: This connector provides a connection to the serial NMEA output, and provides a connector for (re)programming the GPS module.

Pin	Assignment
1	Serial transmitting pin to transmit the NMEA data sentences with 115200 baud.
2	Ground
3	Serial receiving pin to (re)program the GPS module
4	Analog output 1: 0...5.12V, R_i = 1kΩ, $T_{update} \geq 0.3$ms
5	Analog output 2: 0...5.12V, R_i = 1kΩ, $T_{update} \geq 0.3$ms

USBDL1 A16 (1st generation)

The data logger USBDL1 A16 can acquire up to 16 voltage signals. It can also use its first digital channel for signal output.

Figure 8: Data logger USBDL1 A16.

Digital Output Signal

If digital channel 1 is not used as signal input, it can be used as signal output:

Frequency signal ($f_{Min} < f_{Max}$): The output voltage level (TTL, CMOS) is either 0 V or 5 V. The frequency output may lie within the range from 2 Hz to 100 kHz.

PWM signal ($f_{Min} = f_{Max}$): The output voltage level (TTL, CMOS) is a frequency signal 0 V or 5 V with a frequency of f_{Min}, and a duty cycle depending on the signal source and assignment.

Switch state ($f_{Min} > f_{Max}$): The output voltage level (TTL, CMOS) is either 0 V or 5 V depending on the signal source and assignment.

Deviating Technical Data

Property	Description
Box size without plugs, sockets, buttons and sliders:	85 mm × 60 mm × 26 mm
Weight:	0.155 kg

Pin Assignment

PWR/CAN1: This plug supplies the data logger with voltage and connects the data logger to CAN1.

Pin	Assignment	Old Wire Color	Wire Color
1	Supplying voltage U_B (8 V to 16 V DC inverse-polarity protected)	Red	Brown
2	Ground	Brown	White
3	CAN_L (CAN1)	Black	Blue
4	CAN_H (CAN1)	Orange	Black

ON/CAN2: This plug provides a power control input and connects the data logger to CAN2.

Pin	Assignment	Old Wire Color	Wire Color
1	Power control input (6 V to 16 V DC)	Red	Brown
2	Ground	Brown	White
3	CAN_L (CAN2)	Black	Blue
4	CAN_H (CAN2)	Orange	Black

RS232/GPS: This plug provides two serial ports.

Pin	Assignment	9-pin SUB-D plug of host PC
1	TX1	Pin 2
2	Ground	Pin 5
3	RX1	Pin 3
4	U_B – 0.5 V or TX2	RS232 switch up: U_B – 0.5 V RS232 switch down: TX2
5	RX2	

AIN1+2, ..., AIN15+16: These sockets provide inputs for the voltage input signals.

Pin	Assignment
1	U_B – 0.5 V
2	Ground
3	Analog input 1 (or 3/5/7/9/11/13/15)
4	Analog input 2 (or 4/6/8/10/12/14/16)
5	5.12 V reference voltage (max. 50 mA for AIN1+2...AIN15+16)

F1 (I/O): This socket provides a connection to the first digital channel.

Pin	Assignment
1	U_B – 0.5 V
2	Ground
3	Digital input 1 connected over 100 kΩ to 5 V
4	Digital output 1 (= frequency output)

FIN2+3: This socket provides a connection to two digital (frequency) signals.

Pin	Assignment
1	U_B – 0.5 V
2	Ground
3	Digital input 2 connected over 100 kΩ to 5 V
4	Digital input 3 connected over 100 kΩ to 5 V

FIN4+5: This socket provides a connection to the last two digital (frequency) signals.

Pin	Assignment
1	U_B – 0.5 V
2	Ground
3	Digital input 4 connected over 100 kΩ to 5 V
4	Digital input 5 connected over 100 kΩ to 5 V

USBDL1 (2nd generation)

The 2nd generation of the *USBDL1* and all of its subtypes (such as *USBDL1 FD*, *USBDL1 G*, *USBDL1 GA*, *USBDL1 GN*, *USBDL1 GNA*, and *USBDL1 A16*), has additionally a 5-pin socket on its right side. This socket provides up to three digital output channels.

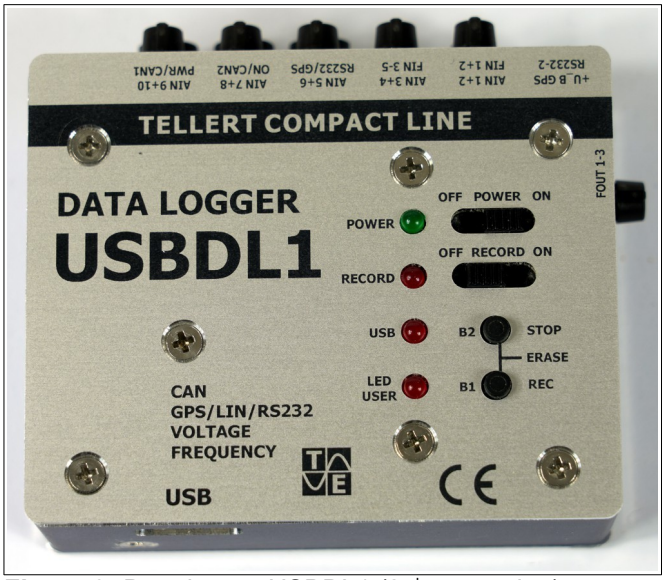

Figure 9: Data logger USBDL1 (2nd generation).

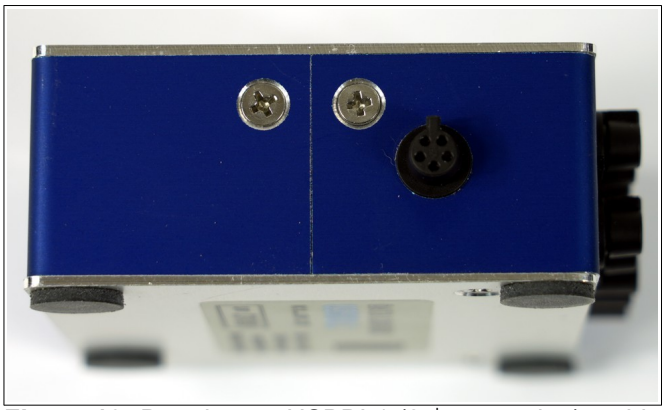

Figure 10: Data logger USBDL1 (2nd generation) – side view.

Digital Output Signal

If the corresponding digital input channel is not used as signal input, it can be used as signal output:

Frequency signal ($f_{Min} < f_{Max}$): The output voltage level (TTL, CMOS) is either 0 V or 5 V. The frequency output may lie within the range from 2 Hz to 100 kHz.

PWM signal ($f_{Min} = f_{Max}$): The output voltage level (TTL, CMOS) is a frequency signal 0 V or 5 V with a frequency of f_{Min}, and a duty cycle depending on the signal source and assignment.

Switch state ($f_{Min} > f_{Max}$): The output voltage level (TTL, CMOS) is either 0 V or 5 V depending on the signal source and assignment.

Deviating Pin Assignment

FOUT1-3: This socket provides a connection to the three digital output signals.

Pin	Assignment
1	Digital output 1 (= frequency output)
2	Digital output 2 (= frequency output)
3	Digital output 3 (= frequency output)
4	N/A
5	Ground

